

## Claims

What is claimed is:

- 1 1. An apparatus comprising:
  - 2 variable delay generator logic configured to generate a signal to cause the
  - 3 presentation of a target an unpredictable time interval after receiving a start
  - 4 signal;
  - 5 presentation duration control logic configured to cause the target presentation to
  - 6 continue for one of an unpredictable presentation time interval determined by
  - 7 the variable delay generator logic, and a selectable predetermined time interval;
  - 8 and
  - 9 presentation count control logic configured to cause target presentation to repeat for
  - 10 one of an unpredictable presentation count determined by the variable delay
  - 11 generator logic, and a selectable predetermined presentation count.
- 1 2. The apparatus of claim 1, further comprising:
  - 2 the variable delay generator logic comprising a first counter configured to count at a
  - 3 first rate, and a second counter configured to count at a second rate starting
  - 4 from an initial count value provided by the first counter, wherein the second
  - 5 counter generates the signal to cause the presentation of the target an
  - 6 unpredictable time interval after receiving the start signal.

1    3. The apparatus of claim 2, the presentation duration control logic comprising a third  
2    counter and configured to provide to the third counter an initial count value determined  
3    from one of the variable delay generator logic and an analog switch.

1    4. The apparatus of claim 3, further comprising:  
2        the presentation duration control logic configured to provide to the third counter an  
3        initial count value provided by the first counter.

1    5. The apparatus of claim 2, the presentation count control logic comprising a third  
2    counter and configured to provide to the third counter a target presentation count  
3    determined from one of the first counter of the variable delay generator logic and an  
4    analog switch.

1    6. The apparatus of claim 1, further comprising:  
2        the variable delay generator logic configured to generate the signal to cause the  
3        presentation of the target after an interval of time comprising a predetermined  
4        delay interval and an unpredictable delay interval.

1    7. The apparatus of claim 1, further comprising:  
2        start/repeat logic to repeatedly generate the start signal a number of times determined  
3        by the presentation count control logic.

1    8. A target controller comprising:  
2        a first counter configured to count at a first rate;  
3        a second counter configured to count at a second rate;

- 4       the first and second counter cooperating to determine a delay between receipt of a
- 5               start signal and target presentation;
- 6       a third counter to determine a target presentation duration; and
- 7       a fourth counter to determine a target presentation count.

1        9. The target controller of claim 8, configured to provide the third counter  
2                with an initial count value selected from one of the count value of  
3                the first counter and a set of selectable fixed values.

1        10. The target controller of claim 8, configured to provide the fourth counter  
2                with an initial count value selected from one of the count value of the first  
3                counter and a set of selectable fixed values.

1        11. A target controller comprising:  
2                a first counter configured to count at a first rate;  
3                a second counter configured to count at a second rate;  
4                the first and second counter cooperating to determine a delay between  
5                receipt of a start signal and target presentation;  
6                a presentation duration control having a setting determined by one of the  
7                first and second counters; and  
8                a presentation count control having a setting determined by one of the first  
9                and second counters.